LT1575 UltraFast Linear Controller Makes Fast Transient Response Power Supplies

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Introduction

The current generation of microprocessors places stringent demands on the power supply that powers the processor core. Allowable supply voltage variations are as low as ±100mV and transient currents are in the range of 5A with 20ns rise and fall times. These requirements demand very accurate, very high speed regulators. The linear solutions employed to date rely on monolithic regulators or PNP transistors driven by low cost control circuits. Because, under the best of circumstances, the response times of these circuits to transient loads are measured in microseconds, these solutions depend on the presence of several hundred microfarads of low ESR decoupling capacitance surrounding the CPU. The cost of these capacitors is a significant percentage of the total power supply cost.

The LT®1575 is an UltraFast™ linear controller that drives a low cost, N-channel, power MOSFET pass transistor and does so with sufficient bandwidth that the bulk decoupling can be *completely* eliminated. As an example, a 200MHz Pentium® processor can operate with only the twenty-four 1µF ceramic capacitors that Intel already requires for the microprocessor. The design uses no tantalum or aluminum electrolytic capacitors on the output. By selecting a sufficiently low on-resistance FET, the dropout voltage of the regulator can be made arbitrarily low. In general, the best performance is obtained with the highest on-resistance (hence, lowest cost) FET that will meet the dropout requirement. Overall system cost and parts count are significantly reduced compared to competing solutions. Reference accuracy is specified as ±0.6% at room temperature and ±1% over the full operating temperature range. Line regulation is typically unmeasureable and load regulation is approximately 1mV for a 5A load change. The LT1575 permits the addition of no-cost current limiting, provides on/off control and has the ability to incorporate thermal limiting for the cost of an external NTC thermistor. The part is available with adjustable outputs or fixed output voltages, in singles and duals (LT1577).

LT1575 Functional Description

Figure 1 shows a block diagram of the LT1575. The basic control circuit consists of a precision bandgap reference, a high gain, wide bandwidth error amplifier and a high speed, low impedance gate-drive stage. The control circuitry is intended to be powered by a nominal 12V (22V absolute max) supply in a typical application, while a lower supply voltage, typically 5V or 3.3V, is used to provide the main input power. The output can be set to any voltage greater than or equal to the reference voltage by proper selection of the feedback divider resistors. The reference is trimmed to a nominal 1.21V. An internal bias supply regulator ensures that the reference will not drift as the supply voltage varies.

Since the MOSFET pass transistor is connected as a source follower, the power-path gain is much more predictable than that of designs that employ PNP bipolar transistors as pass devices. Also, MOSFETs are very high speed devices and are therefore more suitable than PNPs for a wide bandwidth power stage. Another advantage of the follower design is inherently good line rejection. Disturbances on the input supply are not propagated through to the load.

The output driver is designed to be tolerant of capacitive loads, which is precisely what a MOSFET gate will look like to the driver. Driver output impedance is on the order of 2Ω. If the MOSFET used is a very small geometry device with less than approximately 2000pF gate capacitance, it may prove necessary to add between 2Ω and 10Ω in series with the gate. (See page AN69-7 for details.) The error amplifier has an open-loop DC gain of greater than 80dB

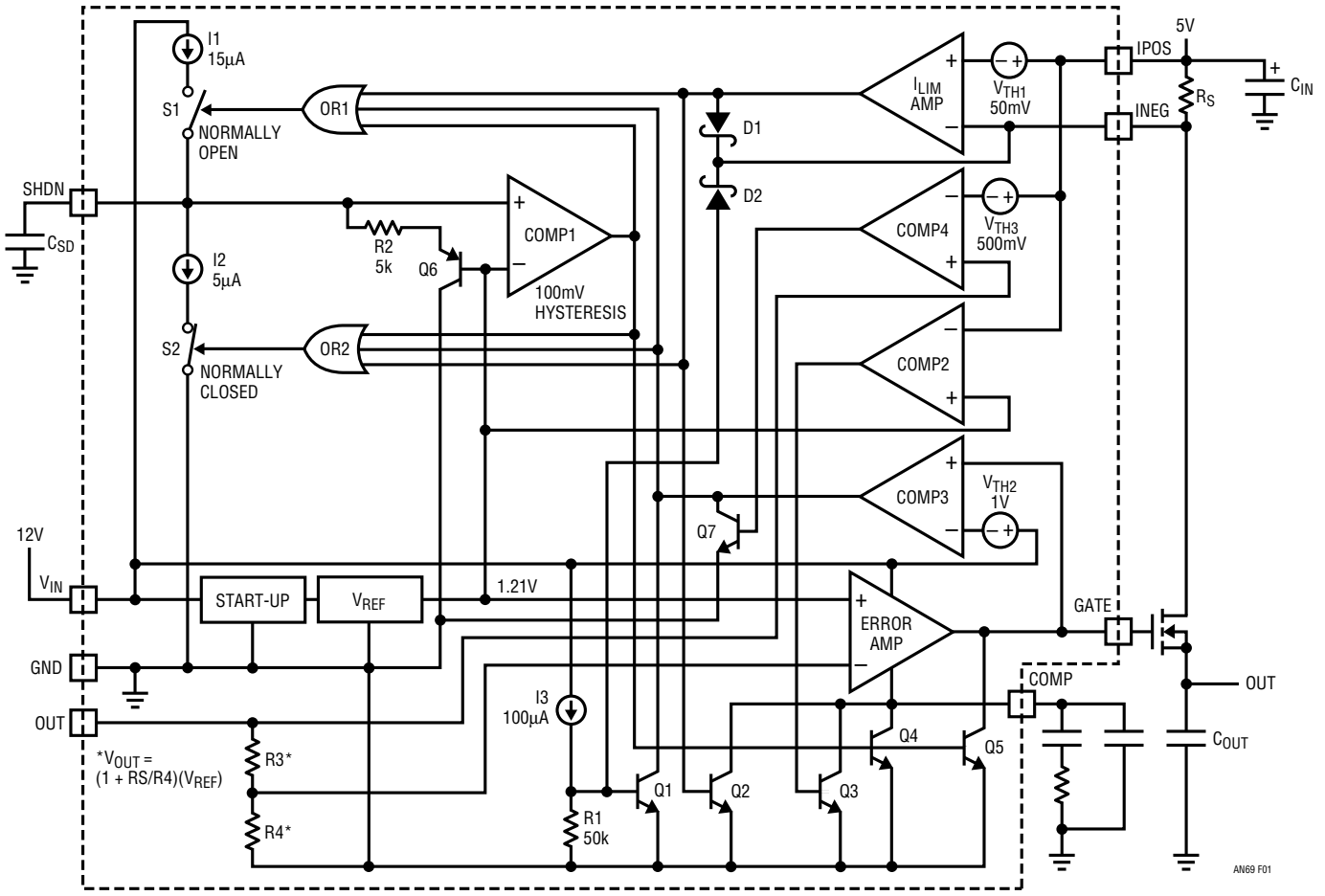

Figure 1. Simplified Circuit of the LT1575

and a typical uncompensated unity-gain frequency of 75MHz. This permits the loop to be crossed over at frequencies on the order of 1MHz and still maintain good phase and gain margins.

Several additional features were included in the design. There are two ways to obtain current limiting. One approach is to add a sense resistor in series with the pass transistor's drain pin to sense load current. The other technique doesn't even need a sense resistor. Let's look at the sense resistor approach first.

The entire load current must flow through the MOSFET drain pin. By connecting a sense resistor between the FET drain and the input supply, the load current can be sensed without reducing the FET's gain. This sense resistor develops a voltage equal to the load current times the sense resistor value. A comparator in the LT1575 looks at the voltage across this resistor, and if this voltage exceeds a 50mV threshold, activates current limit. The 50mV threshold was chosen as a good compromise between low power loss in the sense resistor and reasonable noise immunity.

Several actions are taken when current limit is detected. First, the current limit loop takes control over the output stage. The gate drive voltage is reduced to regulate the current sense voltage to 50mV. In other words, the regulator becomes a current source. Also, referring to Figure 1, current source I2 (5µA sink) turns off and I1 (15µA source) turns on. This starts to charge C_{SD} with approximately 15µA. C_{SD} charges linearly until comparator COMP1 detects that C_{SD}'s voltage has exceeded the 1.21V reference. At this point the chip shuts down, reducing the pass transistor dissipation to zero. This condition is latched. The comparator has approximately 100mV hysteresis to prevent chattering; (this hysteresis is also helpful when using this pin for thermal limit).

There are two ways to restore normal operation after the fault has been cleared. One option is to recycle the input power. The other approach is to pull the Shutdown pin to a voltage below V_{REF}. The time required to latch the output off depends on the value of C1. Use the following formula to select C1: C1 = $(0.012)t_d$, where t_d is delay time in milliseconds and C1 is in μF. By holding shutdown below V_{REF}, the latch-off feature may be disabled and the regulator will continue to output a constant current into a short. This requires being able to sink more than 15μA from the Shutdown pin at less than 1.2V.

The "senseless" current limit technique is activated by grounding Pin 7, the negative current-sense pin. This disables the current limit comparator. A circuit is now enabled (COMP3) that looks at the output driver stage and detects saturation at the positive rail. As soon as saturation is detected, the delay timer is activated, as in the previous case. When the time-out occurs, the output is shut down and latched off. Note that this approach does not limit current while the timer is running. The output current will only be constrained by the input supply and MOSFET limitations. By keeping the timer period short, less than 1ms, the temperature rise in the power FET can be kept under control. Peak currents in this mode of operation may be on the order of 50A to 100A.

There is a slight difference in the operation of this circuit in the fixed-output and adjustable-output versions. In fixed-output parts, comparator, COMP4 of Figure 1, monitors the input/output differential voltage. If this voltage is less than 500mV, the timer will not be allowed to start. This helps prevent false current limit trip-offs caused by turn-on inrush currents, allowing use of a very fast current limit timer. Adjustable parts don't have access to the actual output voltage, only a divided-down version of the output, so this feature is disabled on these devices.

In some cases this can cause a problem. The very large short-circuit currents this circuit can deliver are capable of "dragging down" the input supply in a very short time. The LT1575 undervoltage lockout will then disable the timer and prevent the desired shutdown from occurring.

There are several ways around this problem if it should occur. One solution is to simply set a very short turn-off delay time. As long as the circuit doesn't trip off at turn-on, this is a viable solution. If nuisance tripping at turn-on does occur, two possible solutions exist. The addition of a small RC or a diode/capacitor at the IPOS pin will fix the problem. See Figure 2.

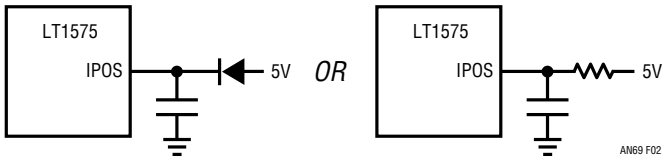

Figure 2. Collapsed-Supply Survival Techniques

The current into IPOS is approximately 1mA. The voltage at IPOS must stay above approximately 2V until the timer shuts the system down. The capacitor value is probably going to be on the order of 5μF to 10μF with the diode circuit for time delays of about 1ms. A low cost aluminum electrolytic capacitor is adequate. The RC circuit won't easily accommodate as long a delay, but for short delays is a little less costly than the diode circuit.

There are no unusual problems related to power sequencing. It makes no difference which supply comes up first. If the 12V supply is late, there is no gate drive available, and thus there is no output. If the main power supply comes up late, there is an undervoltage lockout circuit (COMP2) that ensures that the output remains off until the input rises to approximately 1.2V. Due to the high speed nature of the regulator, turn-on overshoot is virtually nonexistent in a properly designed system.

Typical Applications

Figure 3 shows a typical application circuit. The input voltage is a standard 5V "silver box" and the output is set to 3.50V. This design uses a fixed voltage LT1575 and requires no external feedback divider resistors. Nominal output current is 7A. The current limit of 10A is set by R1, which is a trace on the PC board (see Appendix A for details on designing with trace resistors). The limit need not be very accurate, since the timer circuit will limit temperature rise in the MOSFET. The output filter consists of twenty-four 1μF X7R ceramic, surface mount capacitors. *Proper layout of the decoupling network is crucial to proper operation of this circuit*—see the Board Layout section for details. C7 is set to 0.22μF for approximately 10ms delay time. The MOSFET chosen is an International Rectifier IRFZ24. The specified on-resistance is 0.1Ω and the input capacitance is approximately 1000pF with 1V drain to source. Minimum input voltage for $3.5V_{OUT}$ is determined by the hot on-resistance, which is approximately

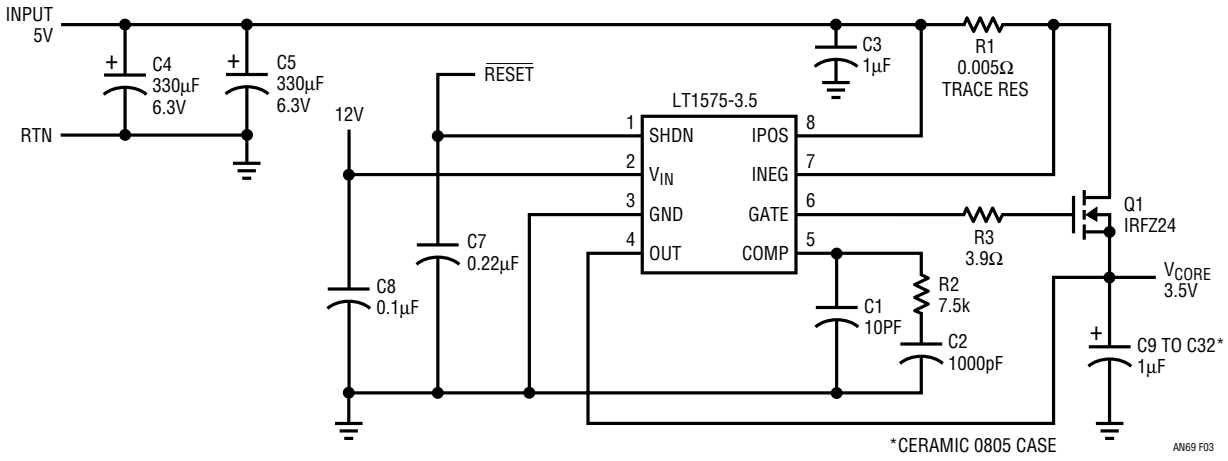

Figure 3. 5V to 3.5V ±100mV Supply

1.5 times the room temperature $R_{DS(ON)}$. The dropout voltage is therefore (0.10Ω)(1.5)(7A) = 1.05V.

Minimum required input voltage is 3.50V + 1.05V = 4.55V.

Figure 4 shows the output voltage transient response to a load step of 200mA to 5A.

Figure 5 shows a circuit that provides a 2.8V output at 5.7A from a 3.3V input. An IRL3303 MOSFET with an on-resistance spec of 0.026Ω is used to meet the low dropout requirement. Decoupling capacitance is the same as in the example above and transient response is similar.

Figure 6 shows the LT1577, a dual regulator. All functions are identical to those of the LT1575. One section is

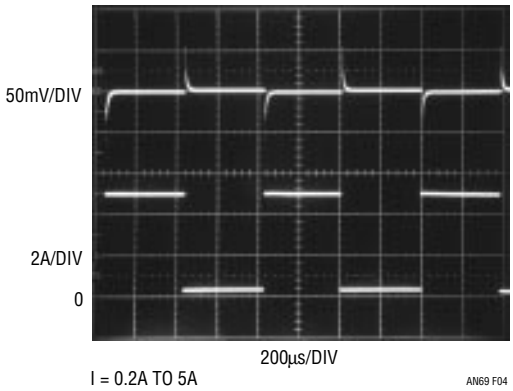

Figure 4. Transient Response

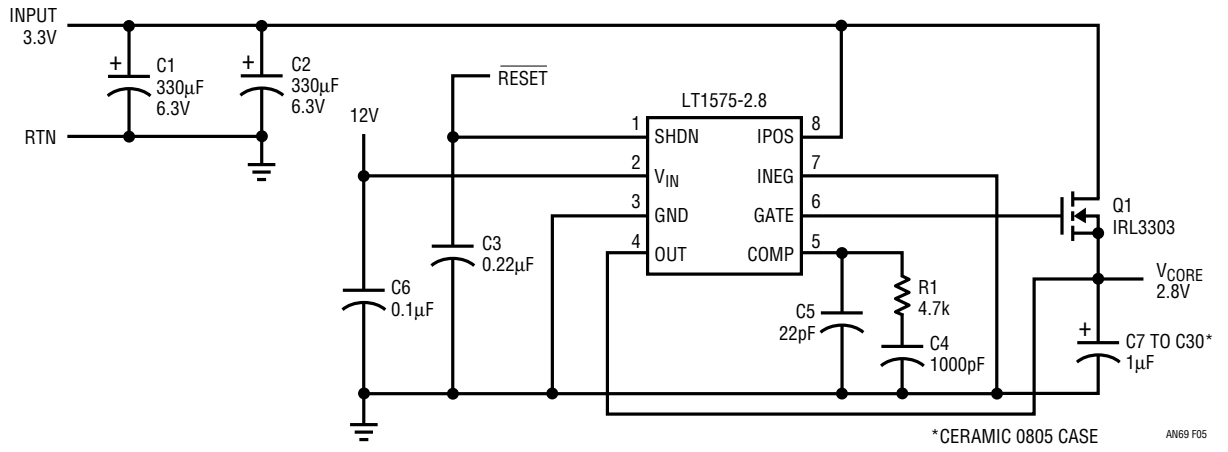

Figure 5. 3.3V to 2.8V ±100mV at 5.7A

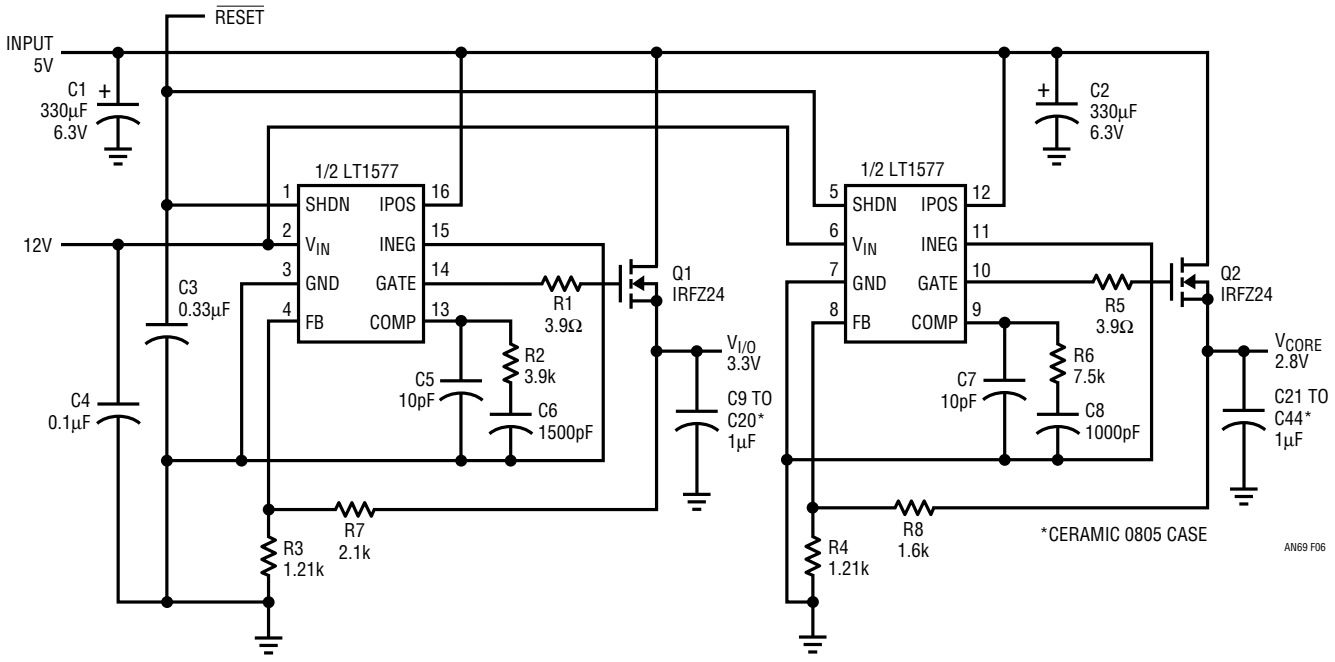

Figure 6. Dual Regulator for "Split-Plane" Systems

configured for a 3.3V output and the other is set up for 2.8V. This circuit provides all the power requirements for a split-plane system: 3.3V for logic and 2.8V for the processor core supply. Both sections use the resistorless current sense for minimum parts count. Note that both Shutdown pins are tied to a common time-delay capacitor. This reduces the charging current from 15µA to 10µA.

If thermal limiting is desired, as might be the case in a relatively low power system that uses a surface mount pass transistor, a low cost NTC thermistor can be configured as shown in Figure 7 or Figure 8. The thermistor used is a Dale NTHS-1206N02. As shown, the trip-off temperature is approximately 120°C for all of these circuits.

In the first case, the design is configured so that the thermal limit will shut the regulator down at 120°C and return to normal operation when the temperature has dropped to approximately 50°C. The regulator will turn back on when the Shutdown pin's voltage has dropped by 100mV. Current limit latch-off is disabled in this case, but if a current sense resistor is employed, current limiting will still be available. The regulator will operate in current limit until the thermal limit is exceeded, then shut off.

Note that the thermistor temperature will be quite a bit lower than the MOSFET tab temperature, even if they are

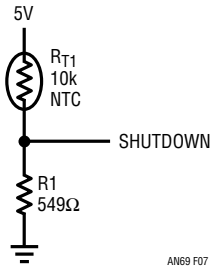

Figure 7. Basic Thermal Limit

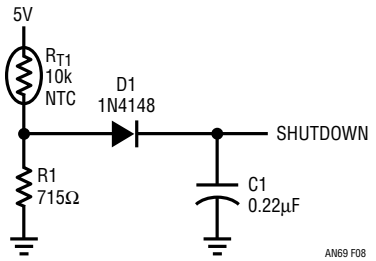

Figure 8. Thermal Limit with Current Limit

in very close physical proximity. It will most likely be necessary to empirically determine the value of the lower divider resistor. This can be done by installing an approximate value for the divider resistor and attaching a thermocouple to the FET drain tab. Run the circuit with normal air

flow and adjust the load current to achieve the desired maximum tab temperature. If the thermal design is good, you may need to disable current limit (short the sense resistor) and operate into a substantial overload to get to the desired temperature. Measure the voltage at the divider center and calculate the thermistor resistance required to produce this voltage. Use this figure to recalculate the divider to get 1.21V across the low leg of the divider at the chosen trip-off temperature.

In the second example, current limit latch-off is enabled, but the accuracy of the temperature limiting suffers due to the variability in the diode V_F. The 1N4148 diode shown here has a V_F of approximately 316mV with a 5μA forward current at 45°C. In this configuration, thermal shutdown is latched off, as is current limit. The Shutdown pin must be pulled low to reenable the supply.

Figure 9 shows an overvoltage protection circuit. If the output exceeds the desired trip level (in this case, 3.36V for a 2.8V supply) the regulator latches off. Current limit latch-off is still functional. Figure 9's circuit could just as easily be connected to the input supply to prevent overheating from excessive input voltage. Figure 10 combines current limit, overvoltage and thermal limiting in one design.

Figure 11 shows how to implement foldback current limiting. A short explanation of the current limit comparator's operation may be helpful. Figure 12 is a simplified schematic of the current limit comparator. The 50mV trip level of the current sense comparator is determined by a 250μA current source and a 200Ω internal resistor in series with the IPOS pin. This current does not flow through the INEG pin. If resistors are added in series with the current sense inputs, they will alter the nominal current sense trip level slightly. Any resistance in series with IPOS will increase the trip threshold by an amount equal to 250μA times R. This can be used to raise the trip threshold above 50mV if desired. The foldback circuit design minimizes alteration of the current limit threshold by keeping the series resistance low (in this case, 10Ω). The two 1N4148 diodes generate an offset voltage of approximately 1.4V so that with a normal input/output differential, the current limit onset is not significantly altered.

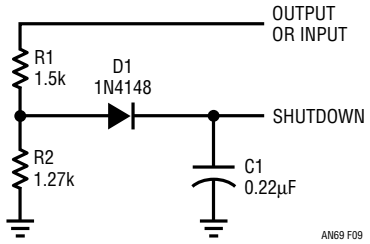

Figure 9. Overvoltage Shutdown

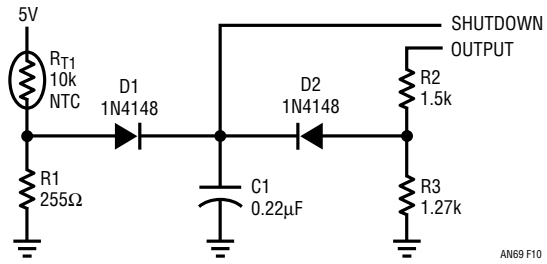

Figure 10. Overvoltage, Thermal Limit with Current Limit

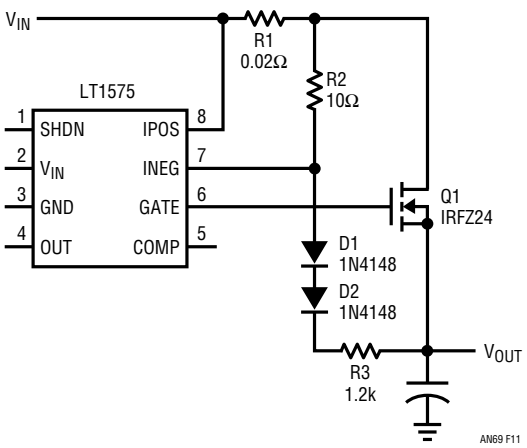

Figure 11. Foldback Current Limit Circuit

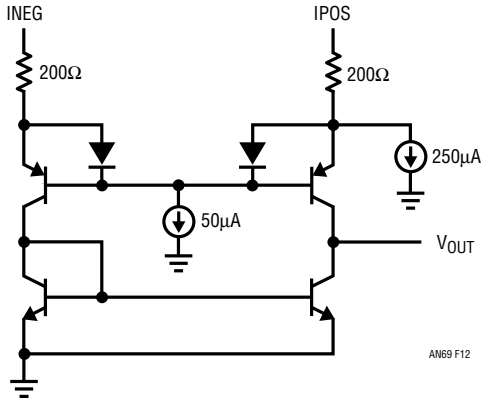

Figure 12. Current Sense Comparator

With V_{IN} = 5V and V_{OUT} = 2.8V, the nominal current through R3 will be quite small, as long as the full output voltage is present. However, when an overload exists, the output voltage falls at the onset of current limit, causing more current to flow through R3. This produces a small offset voltage across the 10Ω resistor. In a hard short, this offset is approximately 30mV; therefore, the voltage across the current sense resistor need only be 20mV instead of 50mV to hold the regulator in current limit. As such, the short-circuit current limit is only 40% of the maximum current. The power dissipation of the pass transistor is greatly reduced with this current limit technique. Figure 13 shows the measured current limit curve for this circuit. Be careful using foldback with nonlinear loads such as lamps or current sources. It is possible for such loads to cause the regulator to get stuck at less than full output voltage.

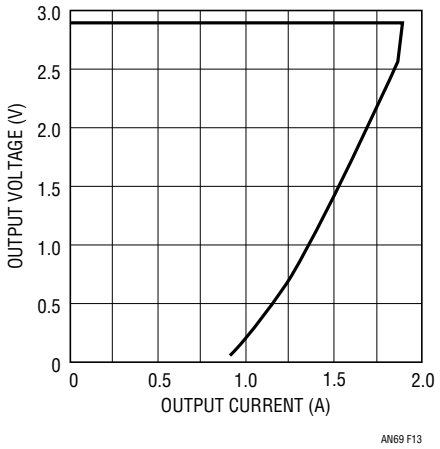

Figure 13. Foldback Current Limit

High Speed Considerations and Component Selection

The secret to success for an LT1575-based design is the ability to achieve very high speed closed-loop performance. As usual, Murphy's law conspires to make life more difficult than we would like. The parasitic elements contained in the PC board traces, as well as the circuit components themselves, conspire to degrade performance. If these parasitics are not properly managed, circuit operation may be disappointing. A good understanding of the critical circuit elements is essential. The following brief tutorial explains the major concerns.

In order to obtain high speed transient response, the LT1575 must develop a large voltage slew rate on the FET gate. The key parameter for FET selection is the FET's transconductance, g_{fs}. The higher this number, the less the total gate voltage excursion required to force a given change in output current; therefore, high gain devices are desired. The FET's input capacitance, C_{ISS}, is less critical. The LT1575's ultimate slew rate will generally be limited by the loop compensation, not the output stage's load capacitance. In tests of typical applications, it was found that a FET with very high gate capacitance and high transconductance will be faster to respond than a very low capacitance device with low transconductance. Higher speeds can generally be obtained from logic-level FETs than from conventional parts. This is due to the much higher g_{fs} specification of logic-level parts.

To reduce cost, select the MOSFET with the highest on-resistance that will meet the dropout specification of the system. There is an inverse relationship between on-resistance and die size. The lower the $R_{DS(ON)}$ specification, the larger the die. More silicon will typically cost more money. For most 5V input to 3.3V or 3.5V output designs, a 0.1Ω MOSFET is sufficient. A standard threshold device such as an IRFZ24 has been shown to be adequate for powering most current-generation processor loads. If faster response is desired, the logic-level IRLZ24 or IRL3303 may be substituted.

MOSFET transconductance is not generally specified at current levels useful for these applications. It may be necessary to calculate a more realistic number from the transfer characteristics of the FET at the current level of interest. A transfer curve plots drain current on the Y-axis against gate source voltage on the X-axis. Find the points on the curve that correspond to the minimum and maximum load conditions. The average incremental transconductance over the load range is $\Delta I_D/\Delta V_{GS}$. The gate voltage will need to change by ΔV_{GS} as the load increases from minimum to maximum. To estimate the slew rate of the LT1575, assume a maximum current out of the COMP pin of approximately 775μA. The slew rate will be 775μA/C_{COMP}, where C_{COMP} is the capacitance from the COMP pin to ground. If there is a series RC to ground, it may be necessary to consider this in the calculation. As long as $\Delta V_{GS}/R_{COMP}$ is much less than 775μA, the series RC can be ignored.

Be sure to look for very high frequency gate oscillations. Small MOSFETs are the most susceptible to this problem. Monitor the gate voltage with an oscilloscope and vary the

load from zero to full load. Look for oscillations in the range of 2MHz to 10MHz. Figure 14 shows an example of a gate oscillation. If such oscillations appear, add a small resistor in series with the FET gate. Start with about 2Ω and gradually increase the value until the oscillations stop. It would be wise to increase the resistor value at least 50% to ensure design margins. It may be possible to reoptimize the loop compensation after adding the gate resistor. The value of the capacitor from COMP to ground (C1 in Figure 3) may be reduced somewhat, since the gate resistor lowers the high frequency gain of the loop.

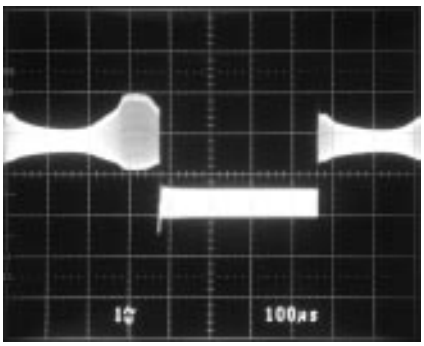

Figure 14. Example of a Gate Oscillation

The MOSFET exhibits several nanohenries of inductance, which appear in series with the device's source and drain leads. The source inductance is by far the most critical. This inductance acts as ballast to degenerate the circuit's high frequency gain. Unfortunately, there isn't anything the user can do to minimize the internal package inductance of the MOSFET. Be careful, however, to minimize the total inductance of the power trace between the FET and the output decoupling capacitors. It appears in series with the internal inductance and must be carefully controlled. Be sure to connect the feedback divider after this inductance, close to the load rather than close to the FET source. Place the FET as close to the load capacitors as possible, and therefore as close to the processor as possible. Unsatisfactory results will be obtained if the FET is placed more than a few centimeters from the load. The additional inductance in the power path will force a significant reduction in the loop crossover frequency to maintain stability. Also, be sure to run a wide (at least 2cm) plane from the FET to the load.

Capacitor selection is very important for proper CPU operation. The load decoupling capacitors must be low impedance devices. They must exhibit minimum levels of ESR (equivalent series resistance) and ESL (equivalent series inductance). Test results on a cleanly laid out board with a 5A load step produced the following data:

Table 1

NUMBER OF CAPACITORS	ΔV FOR 5A LOAD STEP
12	85mV
16	70mV
20	60mV
24	50mV

This test used 1µF, 0805 case surface mount capacitors with X7R dielectric material. Ceramics such as Y5V or Z5U exhibit horrible temperature and bias voltage coefficients. Because there is no bulk capacitance in LT1575 applications, the feedback-loop phase and gain characteristics are largely determined by the value of these capacitors. If the capacitance value changes radically as a function of operating parameters, the chances of loop oscillation increase. In applications where the capacitor temperature is less than 45°C, the low cost Y5V ceramic is adequate. If the temperature is expected to be substantially greater than that, the temperature stability of the X7R material makes it the best choice. The 0805 case parts are also more cost effective than the 1206 case 1µF capacitors. It is preferable to use a large number of low value capacitors in parallel rather than a few larger value parts. The ESR and ESL do not scale with the capacitance and these parasitics will be the parameters that largely control the design. For less demanding applications, it may prove cost effective to use 0.47µF capacitors rather than 1µF. The cost per capacitor is less and the performance hit will not be as large as might be expected. For very cost sensitive applications it may be possible to use Y5V or Z5U material, but only if the expected temperature excursions are small. The loop gain should also be reduced, since more design margin will be needed to prevent oscillations. Use larger capacitor values and a smaller resistor on the COMP node. The transient recovery speed will be lower than can be achieved with the better X7R capacitors.

Board Layout

PC board layout is another critical consideration. A careful analysis of the circuit's parasitics shows that the stray inductance of the power planes and the decoupling capacitors will introduce a double pole at 1MHz to 1.5MHz. The loop must cross over prior to the frequency of this double pole if it is to be stable. Inadvertently doubling the parasitic inductance will make it impossible to stabilize the loop at a frequency high enough to permit adequate transient response. Moreover, the leading edge of the voltage transient due to nearly instantaneous load changes will have excessive amplitude if total inductance isn't carefully controlled. The importance of clean layout cannot be overemphasized. Fortunately, it is not difficult to achieve the required performance. Any layout that will not work with an LT1575 will probably prove unreliable with any regulator.

It is essential to minimize the stray inductance in the interconnects between the decoupling capacitors and the power planes. It is recommended that the capacitors be connected to power and ground islands brought up into the processor socket cavity. These islands then connect to the inner power and ground planes with a liberal sprinkling of vias. In general, plan on a minimum of two vias per end per capacitor. Therefore, in a 24-capacitor system, there should be a total of 96 vias connecting the decoupling capacitors to the power and ground planes.

If the island approach is not used and vias are connected directly to the capacitors' pads, the connections between pads and vias should be as short as possible. Many board designers like to run a 3mm to 4mm length of trace from a pad to a via for good thermal relief. This is far longer than required and produces much more inductance than can be tolerated. A pair of 0.25mm x 4mm traces used to connect a capacitor to a couple of vias will exhibit approximately 1.6nH of inductance. That's more than the capacitor's own ESL by at least a factor of two. It makes little sense to buy a quality, low ESL capacitor and then hook it up with an unintended inductor. Keep vias tangent to the capacitors' solder pads and use two vias per pad.

The LT1575 should have its Ground pin connected directly to the output ground. Run a trace from the LT1575 Ground pin to the closest edge of the processor socket. Keep the trace width at least 0.8mm wide and no more than 5cm long. The controller's own bypass capacitors, feedback divider return and loop compensation return should all connect directly to the chip Ground pin. Do not just drop these connections into the ground plane at the easiest location. Also, be very careful to keep the gate lead far from the Feedback pin. A very clean, high frequency oscillator can be produced by routing these pins too close together. Maintain a minimum of 3mm spacing between these traces. A bit of ground trace placed between these two signals is advisable.

Loop Compensation

Due to the wide bandwidth of the power stage and error amplifier, care must be taken when compensating the feedback loop. The mathematics of the loop-gain analysis is rather complex and is well beyond the scope of this article. Suffice it to say that rather small parasitic elements will cause migraines for the analytical types. An empirical approach will ensure that the desired performance is achieved. After extensive testing, the following recommendations were developed. These compensation values are reasonably conservative and further optimization is possible. However, it is unlikely that a carefully laid out circuit will oscillate if these guidelines are followed. Refer to the Figure 3 schematic:

Table 2

MOSFET TYPE	g_{fs}	C2	R2	C1	R3
IRFZ24	3.1 S	1500pF	7.5k	10pF	3.9Ω
IRLZ24	5.8 S	1500pF	5.6k	10pF	3.9Ω
IRFZ34	4.2 S	1000pF	6.2k	10pF	0Ω
IRLZ34	5.9 S	1000pF	5.6k	10pF	0Ω
IRFZ44	5.3 S	680pF	5.6k	0pF	0Ω
IRLZ44	8.1 S	1000pF	5.6k	10pF	0Ω
IRL3303	6.4 S	1000pF	4.7k	22pF	0Ω

Transconductance numbers used in the above table are average values obtained from stepping the load from approximately 500mA to 5A. The load was changed and the change in gate voltage recorded. g_{fs} was calculated from the results. Capacitor C2 is in series with resistor R2 from the COMP pin (Pin 5) to ground. C1 is connected directly from the COMP pin to ground. R3 is a series gate resistor connected from the gate-drive pin (Pin 6) to the MOSFET gate lead. All of these compensations assume twenty-four 1μF, 0805 case ceramic capacitors with X7R temperature coefficient.

If a smaller quantity of capacitors is used, the value of R2 can be decreased in proportion to the capacitor decrease. This will prove valid down to approximately 50% of the specified capacitor quantity. For example, if an IRFZ24 MOSFET is used with sixteen capacitors, the value of R2 will be (7.5k)(16/24) = 5.0k. Use only the compensation capacitor values in the table.

The circuit should be tested for transient response performance to ensure proper behavior. In order to get a valid test of the design's performance, it is necessary to generate load steps with fast enough edges to excite the loop beyond the crossover frequency. If the edge rates are too slow, the loop will simply track the disturbance without exhibiting its true high frequency behavior. The load steps produced by commercially available electronic loads are completely inadequate for testing this type of circuit. A fast load step generator, such as Intel's Power Validator, which is designed to simulate Pentium processor type load steps, is required. Another approach is to use a power MOSFET to switch a load resistor into and out of the circuit. The load should consist of several surface mount resistors connected in parallel and then connected in series with the FET, as in Figure 15. Drive the FET gate with a square wave from a low impedance driver. Keep the connections between the load pulse circuit and the board as short as possible. Short foils are best used for these interconnects. The inductance of even short wires is excessively high and will produce a great deal of ringing on the output voltage waveform.

It is also desirable, if the equipment is available, to run Bode plots of the open-loop gain and phase. The design should show a minimum of 45° of phase margin under worst-case conditions to ensure stability.

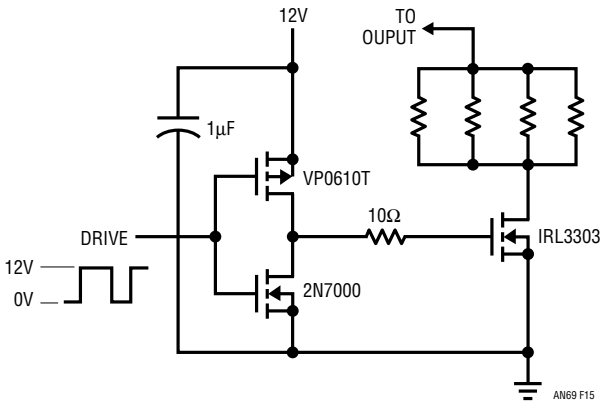

Figure 15. Pulse Generator

Input Filter Considerations

In most 5V input, 3.3V to 3.6V output, monolithic linear regulator designs, the headroom margin is quite small. As a result, a large amount of input filter capacitance is required to ensure that the regulator does not drop out of regulation during a load transient event. Another problem arises because the input source is also likely to be a 5V TTL logic power supply. If large perturbations are induced on the input supply, logic circuits powered by this 5V supply will become unreliable. All of this is still true with LT1575-based designs, but now the designer has an additional option.

Since the dropout voltage of an LT1575-based regulator can be made arbitrarily low by selecting an appropriate MOSFET, the option of adding an input LC filter is now available. Only a very small inductor is required to limit the rate of current rise seen by the input supply. The capacitance on the 5V supply can be greatly reduced as a result of the lowered edge rates. The penalty incurred is a little extra droop at the input to the regulator. However, as was already mentioned, it's a simple matter to meet a lower dropout spec. Figure 16 shows a 5V supply's response to a 5A load step with two 330µF OS-CON capacitors at the regulator input. As would be expected, the instantaneous droop is equal to the capacitor's ESR times the load delta (in this case, $0.015\Omega \times 5A = 75mV$). The MOSFET in this circuit is an IRFZ24. In Figure 17, the MOSFET has been changed to an IRFZ34, which, for a 5A supply, lowers the dropout voltage by about 250mV. A 1µH inductor was added in series with the input supply line, forming an LC lowpass filter. Only one OS-CON capacitor is used on the FET drain. This circuit is shown in Figure 18. The perturbation on the 5V supply is essentially gone. Only the static load regulation error appears on the input supply. The MOSFET drain voltage is now greatly perturbed, as seen in Figure 19. The improved dropout afforded by the larger MOSFET allows for the additional drop at the input without affecting transient response.

The inductor need not be a costly, closed magnetic structure. A very low cost rod core structure is adequate. Magnetic field radiation is limited by the extremely low AC flux swing this type of application induces in the core. In general, this approach can be implemented for the same or slightly less cost than brute force, "throw capacitors at the problem" designs, while affording significantly better system performance.

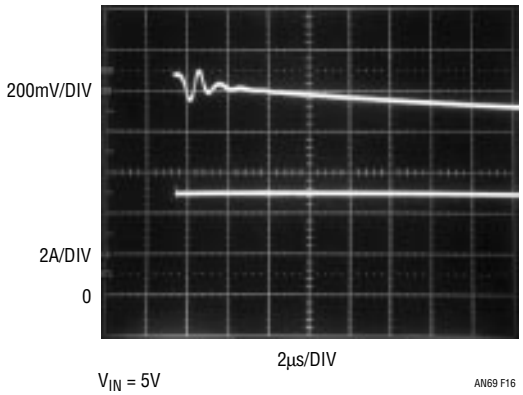

Figure 16. 5V Supply Voltage Ⓐ: Two OS-CONs

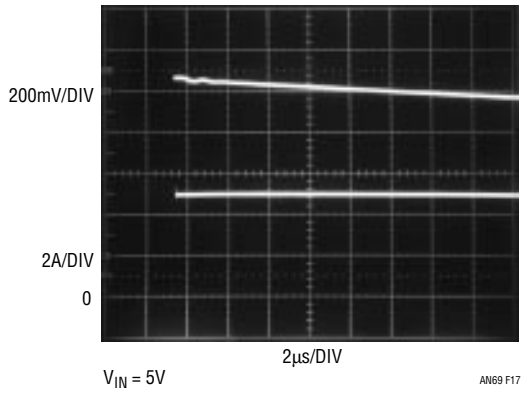

Figure 17. 5V Supply Voltage Ⓐ: One OS-CON + Small Inductor

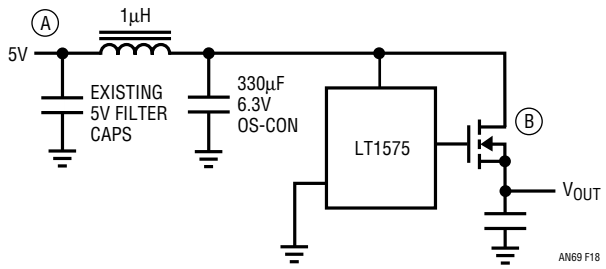

Figure 18. Input Filter Configuration

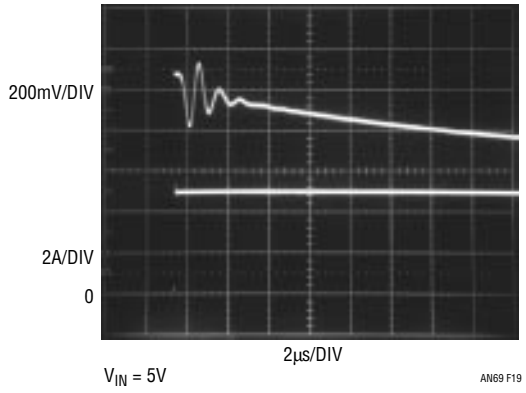

Figure 19. Voltage at FET Drain Ⓑ: One OS-CON + Small Inductor

APPENDIX A

Using PC Board Material as Low Value Resistors

Producing low value resistors for current sense applications is a fairly straightforward process, but a few details must be observed to achieve good results. To obtain the design value of a sense resistor, it is essential that the board's resistivity be well controlled. This is best accomplished by designing the resistors into inner layers rather than outer layers. In a normal board fabrication process, several plating steps deposit additional materials, typically copper and tin, on the outer trace layers. These plating processes are rather poorly controlled. As a result, the resistivity of the outer layers can vary substantially. The inner layers, on the other hand, do not undergo multiple plating operations. The resistivity is quite well defined and is determined largely by the sheet resistance of the starting copper laminate.

The size of the resistance element is determined by several parameters. One must consider the magnitude of the current and the copper sheet thickness to determine the width of the trace. The length is then determined by the desired resistor value.

Recommended Trace Width as a Function of Load Current for a 20˚C Rise

Table A1

	0.5oz Cu	1oz Cu	2oz Cu
1A	0.015" (0.38mm)	0.007" (0.18mm)	0.004" (0.10mm)
2A	0.036" (0.91mm)	0.018" (0.46mm)	0.009" (0.23mm)
4A	0.100" (2.54mm)	0.050" (1.27mm)	0.025" (0.64mm)
6A	0.160" (4.06mm)	0.080" (2.03mm)	0.040" (1.02mm)
8A	0.250" (6.35mm)	0.125" (3.18mm)	0.065" (1.65mm)
10A	0.360" (9.14mm)	0.180" (4.57mm)	0.090" (2.29mm)

After selecting the appropriate trace width from Table A1, calculate the required length using the formula below. This equation assumes a trace temperature of 70°C. Also, a generalized formula is presented to use with an arbitrary sheet thickness and temperature.

$$L = (R_S)(1.667)(T_W)(\rho)$$

where:

L is the trace length

R_S is the desired resistance

T_W is the chosen trace width and

ρ is the sheet weight in oz.

The general equation is:

$$L = \frac{(R_S)(T_W)(S_T)}{R_{CU}\left[1+(T_{MAX}-25°C)(T_C)\right]}$$

where:

S_T is the sheet thickness (mm):

for 0.5oz Cu: S_T = 0.017mm

for 1oz Cu: S_T = 0.034mm

for 2oz Cu: S_T = 0.069mm

T_W is the trace width (mm)

R_{CU} is the resistivity of Cu: 18.22μΩ • mm

T_{MAX} is the maximum trace temperature, °C

T_C is the temperature coefficient of Cu, 0.00393/°C

The calculated length is the mean path length of the trace, in other words, the length measured along the trace center line. A serpentine trace may be used to save space if desired.

The resistor should be tied in to the power plane with multiple vias if it is on a different layer than the plane. The best approach is to use a fairly large diameter via (0.8mm to 1mm). If the solder mask is then pulled back from the edge of the hole, the via will solder fill, allowing quite a bit more current carrying ability than an unfilled hole. Allow 2A/via for filled holes and 1A/via for unfilled holes.

If accuracy is desired, Kelvin sensing must be employed. To do this, extend the resistor beyond the calculated length by approximately 2mm on each end, then add a via inboard from each end of the trace such that the distance between these vias is the calculated length. Connect a signal trace to each via. An alternative is to "T" off of the resistor trace with sense leads. See the following sketches.

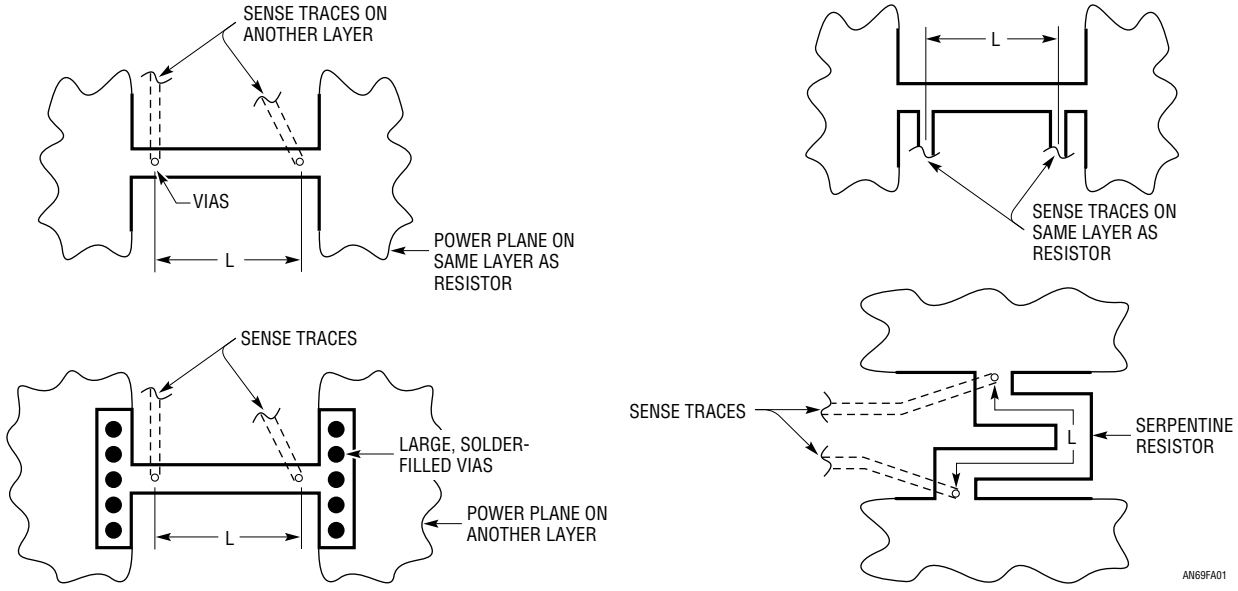

Figure A1. Trace Resistor Configurations

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